Research On Delay-dependent Stability of Parallel DC-DC Converter System Based on a Wireless Communication

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***Abstract*—The current-sharing technology based on Wireless communication allows the current of DC-DC parallel system to be divided equally very well. However, the information transmitted by the network inevitably exist a transmission delay, which makes the traditional system into a time-delay systems. This paper presents a method to comput the Critical Delay of a DC-DC Parallel delay system. The method uses frequency-domain techniques and the DC-DC Parallel System linearized average model to obtain the critical delay. Then a Simulation Model with two parallel modules was built. And the main circuit of the modules is BUCK converter. Finally using the MATLAB simulation tools，we demonstrate the correctness of the method.**

***Index Terms*—time delay; Paralleled DC-DC converters; linearized averaged model; State space equation**

I. INTRODUCTION

At present, in order to meet the application requirements of high-power load, power systems consist of low-power parallel DC-DC converters have been widely used. And the current-sharing technique is the core technology of the parallel DC-DC converter[1-3]. One of the technology is based on the Wireless communication. It uses a communication network to transmit information, without a physical connection between the modules. Various problems caused by the interconnection between the paralleled sub-module and controllers in the power converter can be avoided. So it is widely studied[4-7].

However, when we use the communication network to transmit information, the transmission delay is bound to exist. Communication delays will make the system performance deterioration, even lead to system instability. So do the research on the effect of delay on DC-DC parallel system stability is necessary.

Over the past decades, researchers have a great interest on the delay system stability, and have obtained a series of results on the linear system. But there are very few research on the nonlinear systems. And the methods of them are very complex[8-12].

Although the DC-DC Parallel delay system is nonlinear system, if the power devices of all the converter modules switch periodically, we can use an linearized averaged model to analyze the stability of the system. So this paper presents a theory to analyze the stability of DC-DC converter Delay systems based on literature [11].

Through the simulation we verified the correctness of the proposed method. Compared to the previous literature, this method is simple. It solved the problem of complicated calculation.

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II. THE METHOD OF CALCULATING THE DELAY BOUND

For the system consist of n parallel DC-DC modules, when the power devices of all the converter modules switch periodically, we can use an averaged model to analyze the stability of the system. The state-space averaged model of the system is described by

$$\dot{x}(t) = Ax(t) + A^{'}x(t-\tau) + Bu(t) + B_{rc}V_{ref} \tag{1}$$

where $x(t)$ is the state of the converter. $u(t)$ is the input of the converter，and it is the duty of every switch in the converter. $u(t)$ can be represented by $x(t)$ and $x(t-\tau)$. So system (1) can be expressed as

$$\dot{x}(t) = A_0x(t) + A_1x(t-\tau) + D \tag{2}$$

Theorem： For the system in (2) stable at $\tau = 0$, $A_0 + A_1$ is stable and $rank(A_1) = q$, we define

$$\bar{\tau}_i := \begin{cases} \min\limits_{1\le k\le n} \dfrac{\theta_k^i}{\omega_k^i} & \text{if } \lambda_i(j\omega_k^i I - A_0, A_1) = e^{-j\theta_k^i} \\ & \text{for some } \omega_k^i \in (0,\infty), \theta_k^i \in [0,2\pi] \\ \infty & \text{if } \underline{\rho}(j\omega I - A_0, A_1) > 1, \forall\, \omega \in (0,\infty) \end{cases} \tag{3}$$

Then $\bar{\tau} := \min\limits_{1\le i\le q} \bar{\tau}_i$, and the system in (2) is stable for all $\tau \in [0, \bar{\tau})$ and becomes unstable at $\tau = \bar{\tau}$. In (3),

$$\underline{\rho}(A_0, A_1) = \min\left\{|\lambda| \,\middle|\, \det(A_0 - \lambda A_1) = 0\right\}, \tag{4}$$

and $\lambda(A,B)$ is the generalized eigenvalue of the matrices A and B.

Using the above theorem， we check whether the system is stable independent of delay. We first test the condition

$$\underline{\rho}(j\omega I - A_0, A_1) > 1 \qquad \forall \omega \in (0,\infty). \tag{5}$$

If the condition in (5) is satisfied for all values of ω, then the system is stable independent of delay. If there is some ω for which the condition in (5) is not satisfied, using that value, we solve $\lambda_i(j\omega I - A_0, A_1) = e^{-j\theta}$ for θ and find the corresponding delay using (3).

III. THE BOUND OF A PARALLEL DC-DC BUCK CONVERTER

In order to study the effect of the delay on the system, we take two Buck converters as an example for the simulation. As shown in Figure 1, one of them is master module, the other one is slave module. The control loop of master module includes a voltage loop and a current loop. And the output of the voltage loop act as the reference value for the current loop. The slave module only has a current loop and receives the current reference from the master module. In the voltage loop, the output voltage is compared with a given voltage reference value , then passed through an PI regulator we get the current reference. At the same time, the master module transmit the reference to the slave module through the wireless module. Using their own output current to compare with the reference，then passed through an PI regulator，the slave module gets control variables to adjust the duty of its PWM which is used to control the power MOSFET of the buck converter. So the current will be shared equally.

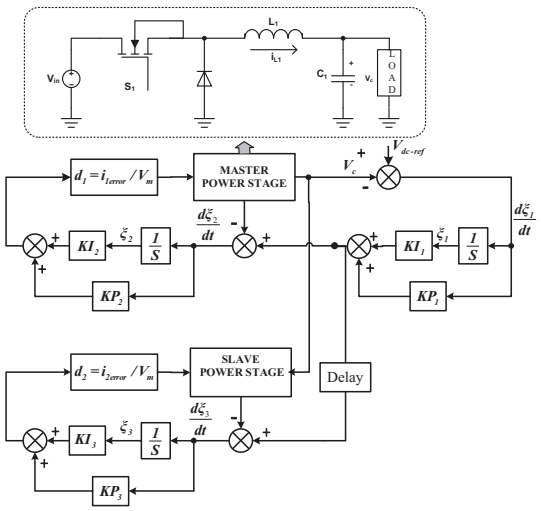


Fig.1. Equivalent block diagram of the dual BUCK parallel system

The state space equation of the system can be described as:

$$\dot{x}(t) = Ax(t) + A'x(t-\tau) + Bu + B_{rc}V_{dc-ref} \tag{6}$$

The state of the converter is

$$x(t) = \begin{bmatrix} i_{L_1} & i_{L_2} & v_c & \xi_1 & \xi_2 & \xi_3 \end{bmatrix}^T \tag{7}$$

where i_{L_1} is the inductor current of master module and i_{L_2} is the inductor current of slave module. v_c is the output voltage of the converter. ξ_1 , ξ_2 , ξ_3 are the intermediate state of the master module voltage loop PI controller, the master module current loop PI controller, the slave module current loop PI controller.

The input of the converter is

$$u(t) = \begin{bmatrix} d_1 & d_2 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{8}$$

where d_1 and d_2 are the duty of master and slave switch signal $d_1 = i_{1error}/V_m$, $d_2 = i_{2error}/V_m$, i_{1error} and i_{1error} can can be represented by $x(t)$ and $x(t-\tau)$. So the above system can be expressed as

$$\dot{x}(t) = A_0 x(t) + A_1 x(t-\tau) + D \tag{9}$$

where D is a constant matrix.

$$A_0 = \begin{bmatrix} -\frac{V_{in}KP_2}{V_m L_1} & 0 & -\frac{1}{L_1} - \frac{V_{in}KP_2KP_1}{V_m L_1} & \frac{V_{in}KP_2KI_1}{V_m L_1} & \frac{V_{in}KI_2}{V_m L_1} & 0 \\ 0 & -\frac{V_{in}KP_3}{V_m L_2} & -\frac{1}{L_2} & 0 & 0 & \frac{V_{in}KI_3}{V_m L_2} \\ \frac{1}{C_1+C_2} & \frac{1}{C_1+C_2} & -\frac{1}{R(C_1+C_2)} & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ -1 & 0 & -KP_1 & KI_1 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{V_{in}KP_3KP_1}{V_m L_2} & -\frac{V_{in}KP_3KI_1}{V_m L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -KP_1 & KI_1 & 0 & 0 \end{bmatrix} \tag{10}$$

For the system described by (9), $rank(A_1) = 1$ and $\bar{\tau} = \tau_1$， To find τ_1 using the criterion in (3), we sweep the frequency from $\infty \rightarrow 0$ and find the points at which $\underline{\rho}(j\omega I - A_0, A_1) \approx 1$. Using this value of ω and the fact that there is only one nonzero generalized eigenvalue for the system considered in this paper, we have $\omega = \omega_1^1$. Next, we find the delay threshold as $\min_{1\le k\le n} \frac{\theta_k^1}{\omega_k^1}$ by varying θ_k^1 in the interval of $[0, 2\pi]$. The parameters for the system are show in Table I.

Using the theorem and MATLAB，we can easily get $\omega = 424$， $\theta = 2.4$， $\bar{\tau} = \frac{\theta}{\omega} = \frac{2.4}{424} \approx 5.66\text{ms}$.

IV. SIMULATION

To verify the validity of the theoretical analysis, we use MATLAB / simulink to build a simulation model. The model is shown in figure 2. Delay module is added to the system to simulate the network transmission delay, the switching frequency is set to 20kHz.

Figure.3 shows the output voltage and inductor current of the network control system at different delay. Figure.3(a) shows that when $\tau = 10ms$ which is much larger than the estimated value, the system failed in parallel. Figure.3(b) shows that when $\tau = 5.6ms$,within the critical range of the estimated value. Although the oscillation amplitude is large, but it is decreases slowly with time, the system will be stable eventually. Figure.3(c) shows that when $\tau = 4ms$ and less than the estimated value, the system starts smoothly and quickly into homeostasis. The simulation results demonstrate that the theory about the delay system is right.

Table I PARAMETERS OF THE MASTER-SLAVE PARALLEL BUCK CONVERTER

Description	Parameter	Value
Input voltage	V_{in}	10V
Output voltage	V_o	5V
capacitance	$C_1 = C_2$	$220\mu F$
inductance	$L_1 = L_2$	$330\mu H$
Load resistance	R	3Ω
PI controller	KP_1	0.28
	KI_1	264
	$KP_2 = KP_3$	0.106
	$KI_2 = KI_3$	410
Ramp height	V_m	1

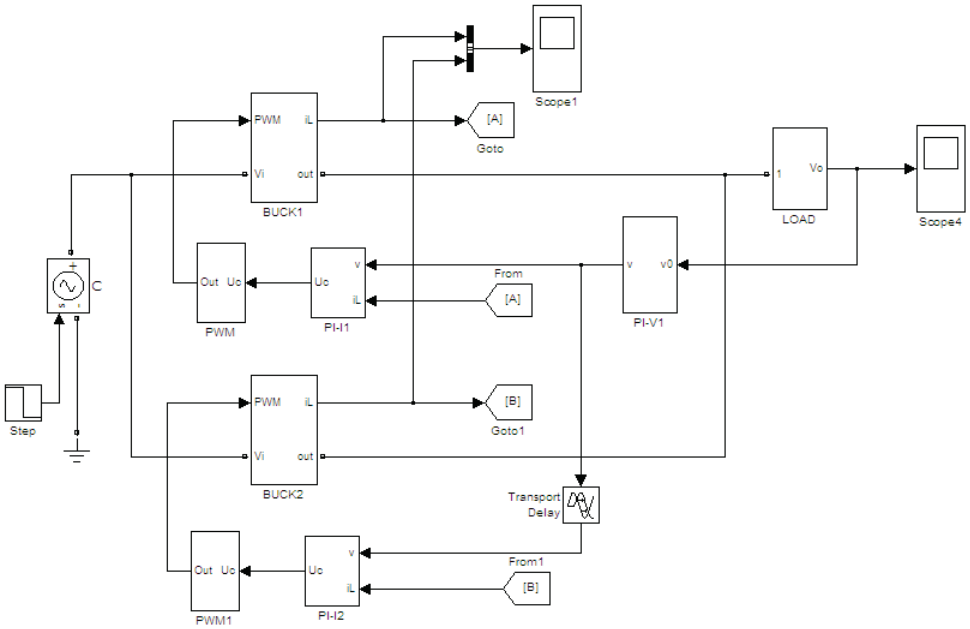
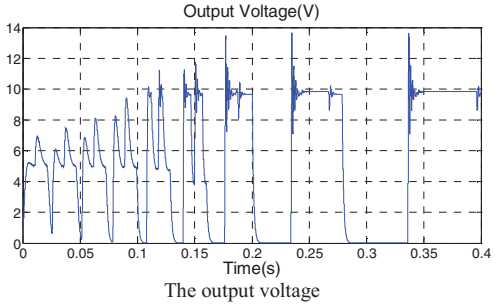
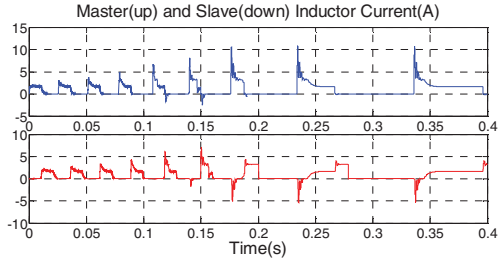


Figure.2. The Matlab simulation model of the paralleled buck

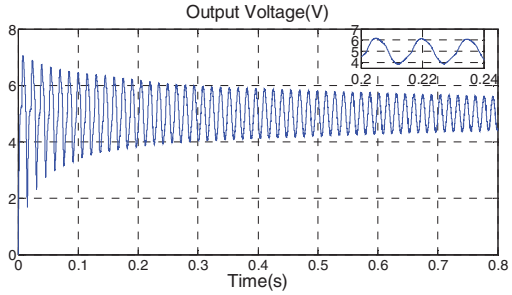


The output voltage

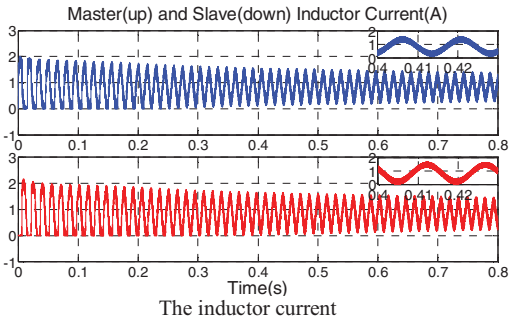


The inductor current

(a) $\tau = 10ms$

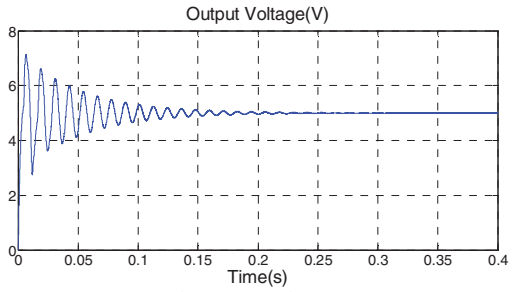


The output voltage

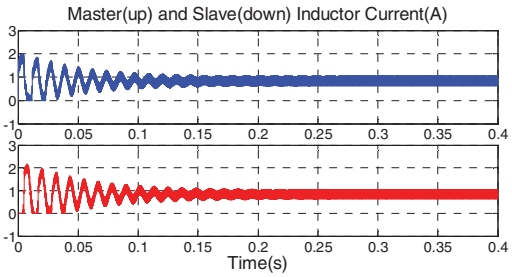


The inductor current

(b) $\tau = 5.6ms$



The output voltage



The inductor current

(c) $\tau = 4ms$

Figure.3. The output voltage and inductor current of the network control system at different delay

V. CONCLUSION

In this paper, we presented a research method on the DC-DC Parallel delay systems. The method is simple. For the example of two parallel BUCK module, we verified the correctness of the method through MATLAB simulation. And from the simulation result we can see when the delay time is slightly less than the calculated threshold delay, the time required for the system to be stable is very long. So delays bounds drawn by the method is large.

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